

Phase-Locked Loop Synthesizer Simulation

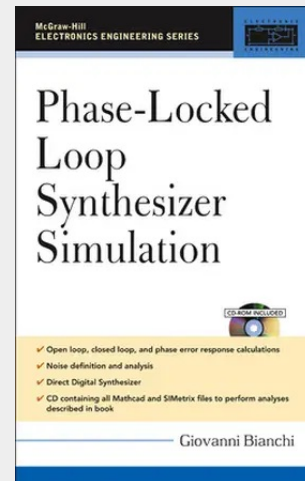
Phase locked loops (PLLs) are electronic circuits that ensure that a communications signal stays locked on a given frequency. Their design is crucial to the workings of wireless communications systems. Virtually all transceivers use PLLs to synthesize the stable, high frequency oscillations necessary for radio & wireless. This book describes how to calculate PLL performances by using standard mathematical or circuit analysis programs. Theoretical descriptions are limited to the minimum needed to explain how to perform calculations. Although presented methods of analysis can be implemented with many commercial programs, their description always refers to Mathcad and SIMetrix.

CD-ROM with analyses in MATHCAD and SIMETRIXA COMPLETE TOOLKIT FOR PLL SYNTHESIZER DESIGNThis book/CD-ROM package provides the analysis and algorithms necessary to perform sophisticated PLL calculations and simulation exercises required for today's advanced communications equipment. Delivering all the tools readers need to begin solving their own design challenges immediately, Phase-Locked Loop Synthesizer Simulation offers:

- Everything necessary to calculate PLL performances with standard mathematical or circuit analysis programs
- A CD with all the book's analyses in MATHCAD and SIMETRIX, with user-variable parameters and configurations
- Minimal theoretical discussion -- only what's needed to explain how to perform calculations
- Open-loop, closed-loop, and phase error response calculations
- Noise definition and response algorithms
- Discussion of direct digital synthesizer
- Methods of analysis that can be implemented with any commercial program, though description always refers to MATHCAD and SIMETRIX

THE DATA NEEDED TO GENERATE PLL SOLUTIONS

- PLL working principles
- Laplace and Fourier transforms
- Transforms of some important functions
- PLL transfer functions
- PLL stability analysis
- PLL order and PLL type
- First-order PLL
- Second-order PLL
- Loop components
- Phase detector
- Multiplier as phase detector
- Phase frequency detector
- Dead zone
- PFD spurs
- Charge pump
- Sampled PLL
- Loop filter
- Reference spur filtering
- Loop filters for voltage output phase detectors
- Loop filters for charge pump
- Loop filter scaling
- VCO
- Frequency dividers
- Frequency divider phase noise
- Fractional-N frequency divider
- Single-accumulator fractional divider
- Multiple-accumulator fractional dividers
- Z transform
- First-order S- ω modulator
- Higher-order S- ω converters
- Synthesizer performance simulation
- Simulation techniques
- Phase noise of PLL synthesizer
- Modulation of the PLL
- Modulation of the reference oscillator only
- Modulation of the VCO only
- Dual-point modulation
- Settling time
- Lock-in
- Pull-in
- PLL performance verification
- Measurement of PLL frequency response magnitude
- Sampling phase detector
- Multiple-loop PLL
- Phase noise of multiple-loop PLL
- Transients in multiple-loop PLL
- Variations on double-loop architecture
- Direct digital synthesizer
- Principle of DDS operation
- Effects of nonideal components on DDS performance
- Enhancements of DDS architecture



100,50 €

93,93 € (zzgl. MwSt.)

Nicht mehr lieferbar

Artikelnummer: 9780071453714

Medium: Buch

ISBN: 978-0-07-145371-4

Verlag: McGraw Hill LLC

Erscheinungstermin: 01.04.2005

Sprache(n): Englisch

Auflage: Erscheinungsjahr 2005

Produktform: Gebunden

Gewicht: 499 g

Seiten: 304

Format (B x H): 160 x 241 mm

