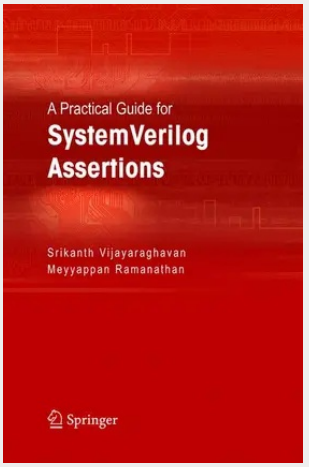
Vijayaraghavan / Ramanathan

A Practical Guide for SystemVerilog Assertions



SystemVerilog language consists of three very specific areas of constructs -- design, assertions and testbench. Assertions add a whole new dimension to the ASIC verification process. Assertions provide a better way to do verification proactively. Traditionally, engineers are used to writing verilog test benches that help simulate their design. Verilog is a procedural language and is very limited in capabilities to handle the complex Asic's built today. SystemVerilog assertions (SVA) are a declarative and temporal language that provides excellent control over time and parallelism. This provides the designers a very strong tool to solve their verification problems. While the language is built solid, the thinking is very different from the user's perspective when compared to standard verilog language. The concept is still very new and there is not enough expertise in the field to adopt this methodology and be successful. While the language has been defined very well, there is no practical guide that shows how to use the language to solve real verification problems. This book will be the practical guide that will help people to understand this new methodology.

"Today's SoC complexity coupled with time-to-market and first-silicon success pressures make assertion based verification a requirement and this book points the way to effective use of assertions."

Satish S. Iyengar, Director, ASIC Engineering, Crimson Microsystems, Inc.

"This book benefits both the beginner and the more advanced users of SystemVerilog Assertions (SVA). First by introducing the concept of Assertion Based Verification (ABV) in a simple to understand way, then by discussing the myriad of ideas in a broader scope that SVA can accommodate. The many real life examples, provided throughout the book, are especially useful."

Irwan Sie, Director, IC Design, ESS Technology, Inc.

"SystemVerilogAssertions is a new language that can find and isolate bugs early in the design cycle. This book shows how to verify complex protocols and memories using SVA with seeral examples. This book is a good reference guide for both design and verification engineers."

Derick Lin, Senior Director, Engineering, Airgo Networks, Inc.

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