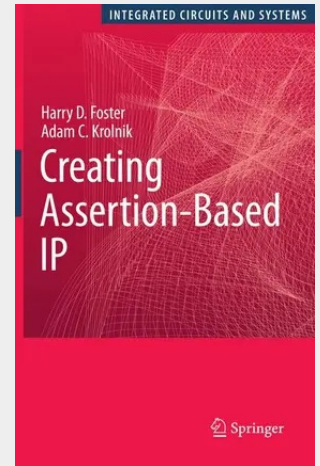


Creating Assertion-Based IP

A project's functional verification testplan is the specification for the verification process. Developing this testplan usually involves the entire engineering team (architects, designers, and verification engineers). This book presents formal testplanning guidelines with examples focused on creating assertion-based verification IP. This is the first book published on this subject. It demonstrates a systematic process for formal specification and formal testplanning, and also demonstrates effective use of assertions languages beyond the traditional language construct discussions. Note that there many books published on assertion languages (such as SystemVerilog assertions and PSL). Yet, none of them discuss the important process of testplanning and using these languages to create verification IP.

Assertion-based IP is much more than a comprehensive set of related assertions. It is a full-fledged reusable and configurable transaction-level verification component, which is used to detect both interesting and incorrect behaviors. Upon detecting interesting or incorrect behavior, the assertion-based IP alerts other verification components within a simulation environment, which are responsible for taking appropriate action. The focus of this book is to bring the assertion discussion up to a higher level and introduce a process for creating effective, reusable, assertion-based IP, which easily integrates with the user's existing verification environment, in other words the testbench infrastructure. The guiding principles promoted in this book when creating an assertion-based IP monitor are: - modularity—assertion-based IP should have a clear separation between detection and action - clarity—assertion-based IP should be written initially focusing on capturing intent (versus optimizations) A unique feature of this book is the fully worked out, detailed examples. The concepts presented in the book are drawn from the authors' experience developing assertion-based IP, as well as general assertion-based techniques. Creating Assertion-Based IP is an important resource for design and verification engineers. From the Foreword: Creating Assertion-Based IP "...reduces to process the creation of one of the most valuable kinds of VIP: assertion-based VIP...This book will serve as a valuable reference for years to come." Andrew Piziali, Sr. Design Verification Engineer Co-Author, ESL Design and Verification: A Prescription for Electronic System Level Methodology Author, Functional Verification Coverage Measurement and Analysis



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