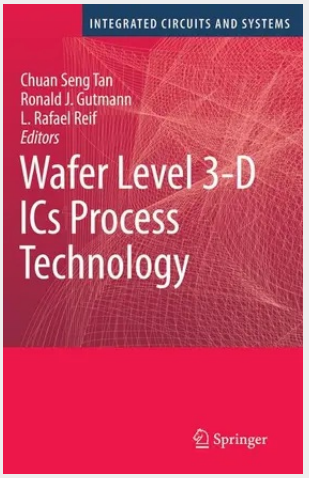
Tan / Gutmann / Reif

Wafer Level 3-D ICs Process Technology



Three-dimensional (3D) integration is clearly the simplest answer to most of the semiconductor industry's vexing problems: heterogeneous integration and red- tions of power, form factor, delay, and even cost. Conceptually the power, latency, and form factor of a system with a ?xed number of transistors all scale roughly linearly with the diameter of the smallest sphere enclosing frequently interacting devices. This clearly provides the fundamental motivation behind 3D technologies which vertically stack several strata of device and interconnect layers with high vertical interconnectivity. In addition, the ability to vertically stack strata with - vergent and even incompatible process ?ows provides for low cost and low parasitic integration of diverse technologies such as sensors, energy scavengers, nonvolatile memory, dense memory, fast memory, processors, and RF layers. These capabilities coupled with today's trends of increasing levels of integrated functionality, lower power, smaller form factor, increasingly divergent process ?ows, and functional diversi?cation would seem to make 3D technologies a natural choice for most of the semiconductor industry. Since the concept of vertical integration of different strata has been around for over 20 years, why aren't vertically stacked strata endemic to the semiconductor industry? The simple answer to this question is that in the past, the 3D advantages while interesting were not necessary due to the tremendous opportunities offered by geometric scaling. In addition, even when the global interconnect problem of high-performance single-core processors seemed insurmountable without inno- tions such as 3D, alternative architectural solutions such as multicores could eff- tivelydelaybutnoteliminatetheneedfor3D.

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