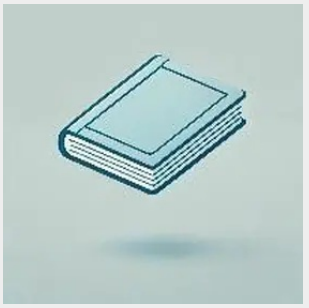
Kumar / Jain

Formal Verification Testbenches

Using Patterns for Reusable and Repeatable VLSI Design Quality



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Formal Verification (FV) has become an essential technology in the verification of IP, core, or SOC design. The authors' previous book, “Formal Verification: An Essential Toolkit for Modern VLSI Design”, offered the definitive guide to design and validation, with advice to help working engineers integrate these techniques into their work. However, understanding the technology is only the beginning: to really use FV effectively, there are many practical considerations in creating effective testbenches. It’s important to use the right formal tools depending on the preferred design style, project phase, and verification goals. Formal Verification Testbenches: Using Patterns for Reusable and Repeatable VLSI Design Quality is designed to provide that guidance, to assist the transition from initial FV usage to FV being the main workhorse of the validation flow. In addition to describing general principles of FV testbench development that apply to any design style, the book takes a deep dive into real testbenches for specific examples: arbiters, sequence controllers, memory controllers, fsm-heavy control blocks, clock gating designs, and dot-product accumulate blocks. It also highlights new opportunities within the field, for example using AI to plan and execute FV. Formal Verification Testbenches: Using Patterns for Reusable and Repeatable VLSI Design Quality enables a design team to confidently plan and execute a project whose primary validation method will be formal verification.

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