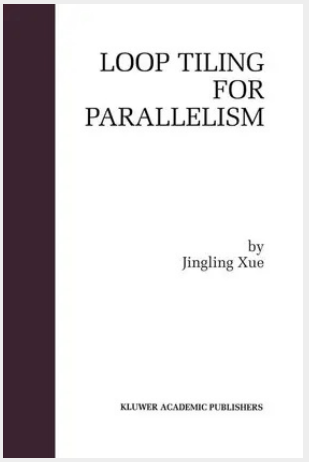
Humana

Loop Tiling for Parallelism



Loop tiling, as one of the most important compiler optimizations, is beneficial for both parallel machines and uniprocessors with a memory hierarchy. This book explores the use of loop tiling for reducing communication cost and improving parallelism for distributed memory machines. The author provides mathematical foundations, investigates loop permutability in the framework of nonsingular loop transformations, discusses the necessary machineries required, and presents state-of-the-art results for finding communication- and time-minimal tiling choices. Throughout the book, theorems and algorithms are illustrated with numerous examples and diagrams. The techniques presented in can be adapted to work for a cluster of workstations, and are also directly applicable to shared-memory machines once the machines are modeled as BSP (Bulk Synchronous Parallel) machines.
Features and key topics:

- Detailed review of the mathematical foundations, including convex polyhedra and cones;
- Self-contained treatment of nonsingular loop transformations, code generation, and full loop permutability;
- Tiling loop nests by rectangles and parallelepipeds, including their mathematical definition, dependence analysis, legality test, and code generation;
- A complete suite of techniques for generating SPMD code for a tiled loop nest;
- Up-to-date results on tile size and shape selection for reducing communication and improving parallelism;
- End-of-chapter references for further reading.

Researchers and practitioners involved in optimizing compilers and students in advanced computer architecture studies will find this a lucid and well-presented reference work with numerous citations to original sources.

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