Krstic

Delay Fault Testing for VLSI Circuits

In the early days of digital design, we were concerned with the logical correctness of circuits. We knew that if we slowed down the clock signal sufficiently, the circuit would function correctly. With improvements in the semiconductor process technology, our expectations on speed have soared. A frequently asked question in the last decade has been how fast can the clock run. This puts significant demands on timing analysis and delay testing. Fueled by the above events, a tremendous growth has occurred in the research on delay testing. Recent work includes fault models, algorithms for test generation and fault simulation, and methods for design and synthesis for testability. The authors of this book, Angela Krstic and Tim Cheng, have personally contributed to this research. Now they do an even greater service to the profession by collecting the work of a large number of researchers. In addition to expounding such a great deal of information, they have delivered it with utmost clarity. To further the reader's understanding many key concepts are illustrated by simple examples. The basic ideas of delay testing have reached a level of maturity that makes them suitable for practice. In that sense, this book is the best x DELAY FAULT TESTING FOR VLSI CIRCUITS available guide for an engineer designing or testing VLSI systems. Tech niques for path delay testing and for use of slower test equipment to test high-speed circuits are of particular interest.

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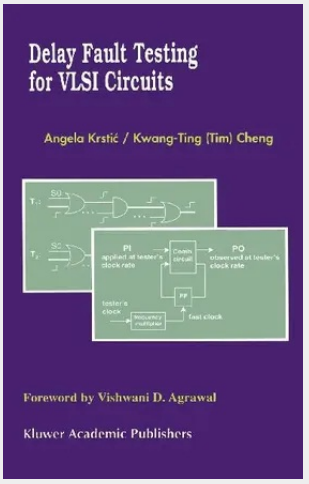

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