

Parallel Algorithms and Architectures for DSP Applications

Over the past few years, the demand for high speed Digital Signal Processing (DSP) has increased dramatically. New applications in real-time image processing, satellite communications, radar signal processing, pattern recognition, and real-time signal detection and estimation require major improvements at several levels; algorithmic, architectural, and implementation. These performance requirements can be achieved by employing parallel processing at all levels. Very Large Scale Integration (VLSI) technology supports and provides a good avenue for parallelism. Parallelism offers efficient solutions to several problems which can arise in VLSI DSP architectures such as:

1. Intermediate data communication and routing: several DSP algorithms, such as FFT, involve excessive data routing and reordering. Parallelism is an efficient mechanism to minimize the silicon cost and speed up the processing time of the intermediate middle stages.
2. Complex DSP applications: the required computation is almost doubled. Parallelism will allow two similar channels processing at the same time. The communication between the two channels has to be minimized.
3. Application specific systems: this emerging approach should achieve real-time performance in a cost-effective way.
4. Testability and fault tolerance: reliability has become a required feature in most of DSP systems. To achieve such property, the involved time overhead is significant. Parallelism may be the solution to maintain acceptable speed performance.

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Kluwer Academic Publishers

106,99 €

99,99 € (zzgl. MwSt.)

Lieferfrist: bis zu 10 Tage

Artikelnummer: 9780792392095

Medium: Buch

ISBN: 978-0-7923-9209-5

Verlag: Humana

Erscheinungstermin: 30.09.1991

Sprache(n): Englisch

Auflage: 1. Auflage 1991

Serie: The Springer International Series in Engineering and Computer Science

Produktform: Gebunden

Gewicht: 1330 g

Seiten: 283

Format (B x H): 160 x 241 mm

