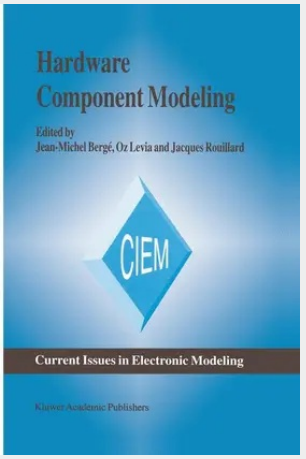
Bergé / Levia / Rouillard

Hardware Component Modeling

The VITAL specification addresses the issues of interoperability, backannotation and high performance simulation for sign-off quality ASIC libraries in VHDL. VITAL provides modeling guidelines and a set of pre-defined packages (containing pre-defined routines for modeling functionality and timing) to facilitate the acceleration of designs which use cells from a VITAL library. The VITAL Level-I guidelines constrain the modeling capabilities provided by VHDL in order to facilitate higher performance (Figure I). Accumulating "gains" Constrained "flexibility" Higher performance & Increased capacity Benefits Flexibility Fujl VHDL 1076 Figure 1: VHDL and VITAL Even within the Level-I guidelines, there are several ways in which a model can be written. In this chapter, we highlight the various modeling trade-offs and provide guidelines which can be used for developing efficient models. We will also discuss the techniques that can be used by tool developers to accelerate the simulation of VIT AL based designs. 2.2. OVERVIEW OF A VITAL LEVEL-I ARCIDTECTURE The VITAL specification is versatile enough to support several modeling styles e.g., distributed delay style, pin-to-pin delay style etc. In general, a VITAL Level-I model can have the structure illustrated in Figure 2.

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