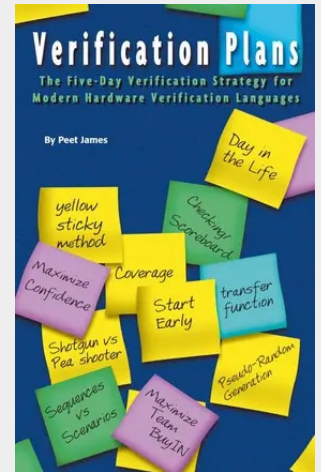


Verification Plans

The Five-Day Verification Strategy for Modern Hardware Verification Languages

Verification is job one in today's modern design process. Statistics tell us that the verification process takes up a majority of the overall work. Chips that come back dead on arrival scream that verification is at fault for not finding the mistakes. How do we ensure success? After an accomplishment, have you ever had someone ask you, "Are you good or are you just lucky?" Many design projects depend on blind luck in hopes that the chip will work. Other's, just adamantly rely on their own abilities to bring the chip to success. In either case, how can we tell the difference between being good or lucky? There must be a better way not to fail. Failure. No one likes to fail. In his book, "The Logic of Failure", Dietrich Dörner argues that failure does not just happen. A series of wayward steps leads to disaster. Often these wayward steps are not really logical, decisive steps, but more like default omissions. Anti-planning if you will, an ad-hoc approach to doing something. To not plan then, is to fail.

The task of verification is always larger than the task of the design effort. Why? Because the verification system has to encompass the entire functionality of the device under verification. It has to mimic the real world environment that the device will actually operate in. It needs to catch functional errors. It needs to give feedback information to guide further verification. The design effort proceeds from a design specification. Verification systems need to proceed from a verification plan. A comprehensive document that describes the verification system and all its components. A plan that details how the verification system will be built. With the advent of hardware verification languages, today's verification systems have grown in complexity making verification plans even more paramount. This book is a practical guide on how to get a verification team jumpstarted into verification success by the joint creation of a verification plan. The book includes: -A detailed five day approach that gives day by day, step by step instructions on how to design and document your verification system. -An introduction to hardware verification languages, their pseudo-random mindset, their enabling methodologies (generation, checking and coverage), and how these effect the development of a verification plan. -Practical guidance in common people issues, formatting decisions and information extraction methods to enhance your verification plan brainstorming sessions. -An appendix full of verification plan examples and support documents.



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