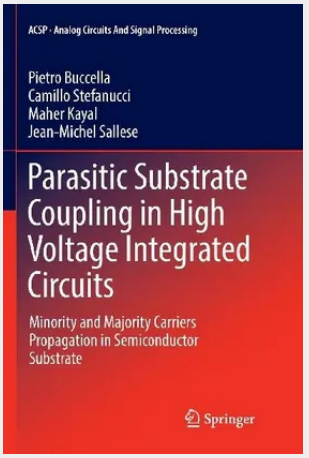
Buccella / Stefanucci / Kayal

Parasitic Substrate Coupling in High Voltage Integrated Circuits

Minority and Majority Carriers Propagation in Semiconductor Substrate



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The injection of majority and minority carriers in the substrate is a recurring problem in smart power ICs containing high voltage, high current switching devices besides sensitive control, protection and signal processing circuits.

The injection of parasitic charges leads to the activation of substrate bipolar transistors. This book explores how these events can be evaluated for a wide range of circuit topologies. To this purpose, new generalized devices implemented in Verilog-A are used to model the substrate with standard circuit simulators. This approach was able to predict for the first time the activation of a latch-up in real circuits through post-layout SPICE simulation analysis.

- Discusses substrate modeling and circuit-level simulation of parasitic bipolar device coupling effects in integrated circuits;
- Includes circuit back-annotation of the parasitic lateral n-p-n and vertical p-n-p bipolar transistors in the substrate;
- Uses Spice for simulation and characterization of parasitic bipolar transistors, latch-up of the parasitic p-n-p-n structure, and electrostatic discharge (ESD) protection devices;
- Offers design guidelines to reduce couplings by adding specific protections.

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106,99 €
99,99 € (zzgl. MwSt.)

Lieferfrist: bis zu 10 Tage

Artikelnummer: 9783030089764
Medium: Buch
ISBN: 978-3-030-08976-4
Verlag: Palgrave Macmillan
Erscheinungstermin: 11.02.2019
Sprache(n): Englisch
Auflage: Softcover Nachdruck of the original 1. Auflage 2018
Serie: Analog Circuits and Signal Processing
Produktform: Kartoniert
Gewicht: 318 g
Seiten: 183
Format (B x H): 155 x 235 mm

Kundenservice Verlag Dr. Otto Schmidt KG
Neumannstraße 10, 40235 Düsseldorf | kundenservice@otto-schmidt.de | 0221-93738-997 (Inland)