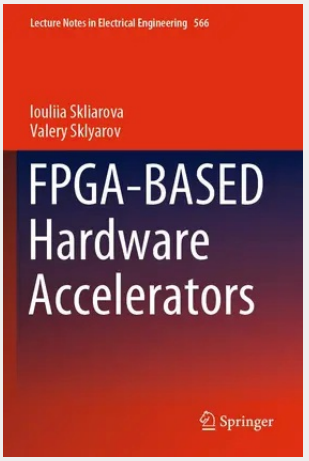
Skliarova / Sklyarov

FPGA-BASED Hardware Accelerators



This book suggests and describes a number of fast parallel circuits for data/vector processing using FPGA-based hardware accelerators. Three primary areas are covered: searching, sorting, and counting in combinational and iterative networks. These include the application of traditional structures that rely on comparators/swappers as well as alternative networks with a variety of core elements such as adders, logical gates, and look-up tables. The iterative technique discussed in the book enables the sequential reuse of relatively large combinational blocks that execute many parallel operations with small propagation delays. For each type of network discussed, the main focus is on the step-by-step development of the architectures proposed from initial concepts to synthesizable hardware description language specifications. Each type of network is taken through several stages, including modeling the desired functionality in software, the retrieval and automatic conversion of key functions, leading to specifications for optimized hardware modules. The resulting specifications are then synthesized, implemented, and tested in FPGAs using commercial design environments and prototyping boards. The methods proposed can be used in a range of data processing applications, including traditional sorting, the extraction of maximum and minimum subsets from large data sets, communication-time data processing, finding frequently occurring items in a set, and Hamming weight/distance counters/comparators. The book is intended to be a valuable support material for university and industrial engineering courses that involve FPGA-based circuit and system design.

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