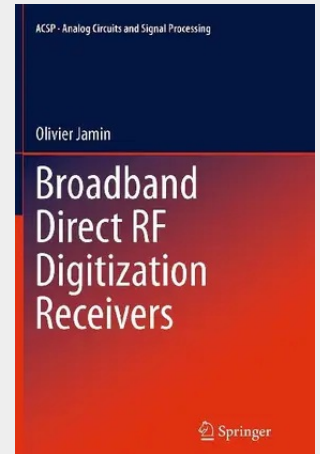


Broadband Direct RF Digitization Receivers

This book discusses the trade-offs involved in designing direct RF digitization receivers for the radio frequency and digital signal processing domains. A system-level framework is developed, quantifying the relevant impairments of the signal processing chain, through a comprehensive system-level analysis. Special focus is given to noise analysis (thermal noise, quantization noise, saturation noise, signal-dependent noise), broadband non-linear distortion analysis, including the impact of the sampling strategy (low-pass, band-pass), analysis of time-interleaved ADC channel mismatches, sampling clock purity and digital channel selection. The system-level framework described is applied to the design of a cable multi-channel RF direct digitization receiver. An optimum RF signal conditioning, and some algorithms (automatic gain control loop, RF front-end amplitude equalization control loop) are used to relax the requirements of a 2.7GHz 11-bit ADC. A two-chip implementation is presented, using BiCMOS and 65nm CMOS processes, together with the block and system-level measurement results. Readers will benefit from the techniques presented, which are highly competitive, both in terms of cost and RF performance, while drastically reducing power consumption.

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