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Languages and Compilers for High Performance Computing

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The 17th International Workshop on Languages and Compilers for High P- formance Computing was hosted by Purdue University in September 2004 on Purdue campus in West Lafayette, Indiana, USA. The workshop is an annual international forum for leading research groups to present their current research activities and the latest results, covering languages, compiler techniques, r- time environments, and compiler-related performance evaluation for parallel and high-performance computing. Eighty-six researchers from Canada, France, Japan, Korea, P. R. China, Spain, Taiwan and the United States attended the workshop. A new feature of LCPC 2004 was its mini-workshop on Research-Compiler Infrastructures. Representatives from four projects, namely Cetus, LLVM, ORC and Trimaran, gavea 90-minute long presentation each. In addition, 29 research papers were presented at the workshop. These papers were reviewed by the p- gram committee. External reviewers were used as needed. The authors received additional comments during the workshop. The revisions after the workshop are now assembled into these ?nal proceedings. A panel sessionwasorganizedby Samuel Midki? onthe questionof “What is GoodCompilerResearch– Theory,PracticeorComplexity?”Theworkshopalso had the honor and pleasure to have two keynote speakers, Peter Kogge of the University of Notre Dame and David Kuck of Intel Inc., both pioneers in high performance computing. Peter Kogge gave a presentation titled “Architectures and Execution Models: How New Technologies May A?ect How LanguagesPlay on Future HPC Systems”. David Kuck presented Intel’s vision and roadmap for parallel and distributed solutions.

Experiences in Using Cetus for Source-to-Source Transformations.- The LLVM Compiler Framework and Infrastructure Tutorial.- An Overview of the Open Research Compiler.- Trimaran: An Infrastructure for Research in Instruction-Level Parallelism.- Phase-Based Miss Rate Prediction Across Program Inputs.- Speculative Subword Register Allocation in Embedded Processors.- Empirical Performance-Model Driven Data Layout Optimization.- Implementation of Parallel Numerical Algorithms Using Hierarchically Tiled Arrays.- A Geometric Approach for Partitioning N-Dimensional Non-rectangular Iteration Spaces.- JuliusC: A Practical Approach for the Analysis of Divide-and-Conquer Algorithms.- Exploiting Parallelism in Memory Operations for Code Optimization.- An ILP-Based Approach to Locality Optimization.- A Code Isolator: Isolating Code Fragments from Large Programs.- The Use of Traces for Inlining in Java Programs.- A Practical MHP Information Analysis for Concurrent Java Programs.- Efficient Computation of Communicator Variables for Programs with Unstructured Parallelism.- Compiling High-Level Languages for Vector Architectures.- HiLO: High Level Optimization of FFTs.- Applying Loop Optimizations to Object-Oriented Abstractions Through General Classification of Array Semantics.- MSA: Multiphase Specifically Shared Arrays.- Supporting SQL-3 Aggregations on Grid-Based Data Repositories.- Supporting XML Based High-Level Abstractions on HDF5 Datasets: A Case Study in Automatic Data Virtualization.- Performance of OSCAR Multigrain Parallelizing Compiler on SMP Servers.- Experiences with Co-array Fortran on Hardware Shared Memory Platforms.- Experiments with Auto-Parallelizing SPEC2000FP Benchmarks.- An Offline Approach for Whole-Program Paths Analysis Using Suffix Arrays.- Automatic Parallelization Using the Value Evolution Graph.- A New Dependence Test Based on Shape Analysis for Pointer-Based Codes.- Partial Value Number Redundancy Elimination.- Overflow Controlled SIMD Arithmetic.- Branch Strategies to Optimize Decision Trees for Wide-Issue Architectures.- Extending the Applicability of Scalar Replacement to Multiple Induction Variables.- Power-Aware Scheduling for Parallel Security Processors with Analytical Models.