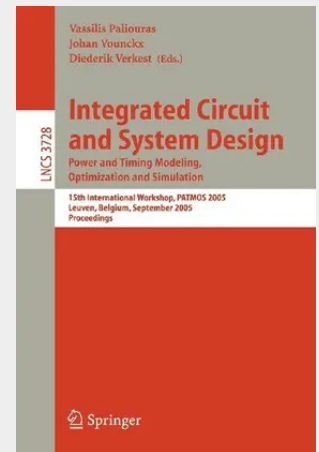


Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation

15th International Workshop, PATMOS 2005, Leuven, Belgium, September 21-23, 2005, Proceedings

Welcome to the proceedings of PATMOS 2005, the 15th in a series of international workshops. PATMOS 2005 was organized by IMEC with technical co-sponsorship from the IEEE Circuits and Systems Society. Over the years, PATMOS has evolved into an important European event, where researchers from both industry and academia discuss and investigate the emerging challenges in future and contemporary applications, design methodologies, and tools required for the development of upcoming generations of integrated circuits and systems. The technical program of PATMOS 2005 contained state-of-the-art technical contributions, three invited talks, a special session on hearing-aid design, and an embedded tutorial. The technical program focused on timing, performance and power consumption, as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis and optimization in the nanometer era. The Technical Program Committee, with the assistance of additional expert reviewers, selected the 74 papers to be presented at PATMOS. The papers were divided into 11 technical sessions and 3 poster sessions. As is always the case with the PATMOS workshops, the review process was anonymous, full papers were required, and several reviews were carried out per paper. Beyond the presentations of the papers, the PATMOS technical program was enriched by a series of speeches offered by world class experts, on important emerging research issues of industrial relevance. Prof. Jan Rabaey, Berkeley, USA, gave a talk on "Traveling the Wild Frontier of Ultra Low-Power Design", Dr. Sung Bae Park, Samsung, gave a presentation on "DVL (Deep Low Voltage): Circuits and Devices", Prof.

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