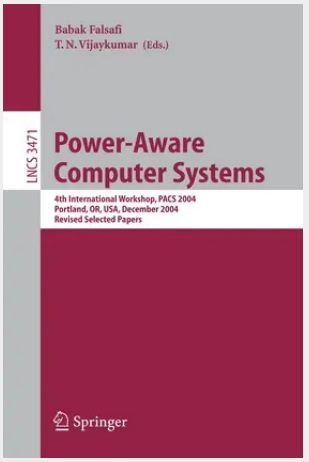
Falsafi / Vijaykumar

Power-Aware Computer Systems

4th International Workshop, PACS 2004, Portland, OR, USA, December 5, 2004, Revised Selected Papers

Welcome to the proceedings of the Power-Aware Computer Systems (PACS 2004) workshop held in conjunction with the 37th Annual International Sym- sium on Microarchitecture (MICRO-37). The continued increase of power and energy dissipation in computer systems has resulted in higher cost, lower re- ability, and reduced battery life in portable systems. Consequently, power and energy have become ?rst-class constraints at all layers of modern computer s- tems. PACS 2004 is the fourth workshop in its series to explore techniques to reduce power and energy at all levels of computer systems and brings together academic and industry researchers. The papers in these proceedings span a wide spectrum of areas in pow- aware systems. We have grouped the papers into the following categories: (1) microarchitecture- and circuit-level techniques, (2) power-aware memory and interconnect systems, and (3) frequency- and voltage-scaling techniques. The ?rst paper in the microarchitecture group proposes banking and wri- back ?ltering to reduce register ?le power. The second paper in this group - timizes both delay and power of the issue queue by packing two instructions in each issue queue entry and by memorizing upper-order bits of the wake-up tag. The third paper proposes bit slicing the datapath to exploit narrow width operations, and the last paper proposes to migrate application threads from one core to another in a multi-core chip to address thermal problems.

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53,49 €
49,99 € (zzgl. MwSt.)

Lieferfrist: bis zu 10 Tage

Artikelnummer: 9783540297901
Medium: Buch
ISBN: 978-3-540-29790-1
Verlag: Springer
Erscheinungstermin: 12.12.2005
Sprache(n): Englisch
Auflage: 1. Auflage 2005
Serie: Theoretical Computer Science and General Issues
Produktform: Kartoniert
Gewicht: 308 g
Seiten: 181
Format (B x H): 155 x 235 mm

Kundenservice Verlag Dr. Otto Schmidt KG
Neumannstraße 10, 40235 Düsseldorf | kundenservice@otto-schmidt.de | 0221-93738-997 (Inland)