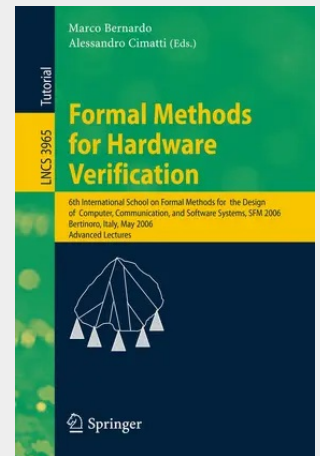


## Formal Methods for Hardware Verification

6th International School on Formal Methods for the Design of Computer, Communication, and Software Systems, SFM 2006, Bertinoro, Italy, May 22-27, 2006, Advances Lectures

This book presents 8 papers accompanying the lectures of leading researchers given at the 6th edition of the International School on Formal Methods for the Design of Computer, Communication and Software Systems (SFM 2006). SFM 2006 was devoted to formal techniques for hardware verification and covers several aspects of the hardware design process, including hardware design languages and simulation, property specification formalisms, automatic test pattern generation, symbolic trajectory evaluation, and more.

high-performance simulation-based model-checking technique called symbolic trajectory evaluation.



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