Falsafi / Vijaykumar

Power-Aware Computer Systems

First International Workshop, PACS 2000 Cambridge, MA, USA, November 12, 2000 Revised Papers

The phenomenal increases in computer system performance in recent years have been accompanied by a commensurate increase in power and energy dissipation. The latter has directly resulted in demand for expensive packaging and cooling technology, an increase in product cost, and a decrease in product reliability in all segments of the computing market. Moreover, the higher power/energy dissipation has signi cantly reduced battery life in portable systems. While - stem designers have traditionally relied on circuit-level techniques to reduce - wer/energy, there is a growing need to address power/energy dissipation at all levels of the computer system. We are pleased to welcome you to the proceedings of the Power-Aware C- puter Systems (PACS 2000) workshop. PACS 2000 was the rst workshop in its series and its aim was to bring together experts from academia and industry to address power-/energy-awareness at all levels of computer systems. In these p- ceedings, we bring you several excellent research contributions spanning a wide spectrum of areas in power-aware systems, from application all the way to c- pilers and microarchitecture, and to power/performance estimating models and tools. We have grouped the contributions into the following speci c categories: (1) power-aware microarchitectural/circuit techniques, (2) application/compiler power optimizations, (3) exploiting opportunity for power optimization in - struction scheduling and cache memories, and (4) power/performance models and tools.

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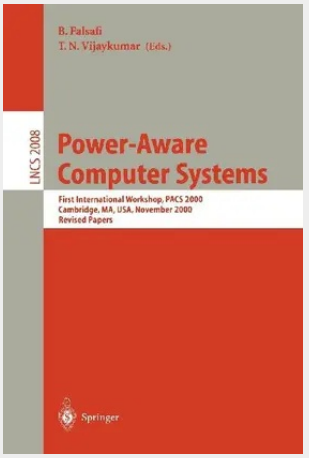

53,49 €
49,99 € (zzgl. MwSt.)

Lieferfrist: bis zu 10 Tage

Artikelnummer: 9783540423294
Medium: Buch
ISBN: 978-3-540-42329-4
Verlag: Springer
Erscheinungstermin: 11.07.2001
Sprache(n): Englisch
Auflage: Erscheinungsjahr 2001
Serie: Lecture Notes in Computer Science
Produktform: Kartoniert
Gewicht: 265 g
Seiten: 158
Format (B x H): 155 x 235 mm

Kundenservice Verlag Dr. Otto Schmidt KG
Neumannstraße 10, 40235 Düsseldorf | kundenservice@otto-schmidt.de | 0221-93738-997 (Inland)