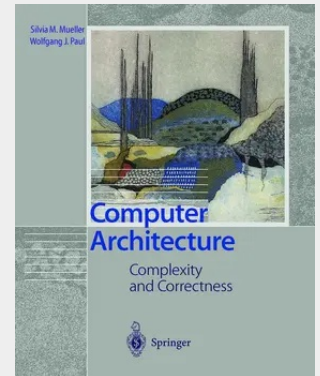


Computer Architecture

Complexity and Correctness

Computer Architecture: Complexity and Correctness develops, at the gate level, the complete design of a pipelined RISC processor with delayed branch, forwarding, hardware interlock, precise maskable nested interrupts, caches, and a fully IEEE-compliant floating point unit. In contrast to other design approaches applied in practice and unlike other textbooks available, the design presented here are modular, clean and complete up to the construction of entire complex machines. The authors' systematically basing their approach on rigorous mathematical formalisms allows for rigorous correctness proofs, accurate hardware costs determination, and performance evaluation as well as, generally speaking, for coverage of a broad variety of relevant issues within a reasonable number of pages. The book is written as a text for classes on computer architecture and related topics and will serve as a valuable source of reference for professionals in hardware design.

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