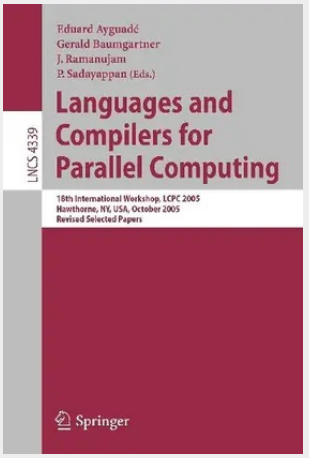
Ayguadé / Baumgartner / Ramanujam

Languages and Compilers for Parallel Computing

18th International Workshop, LCPC 2005, Hawthorne, NY, USA, October 20-22, 2005, Revised Selected Papers



This book constitutes the thoroughly refereed post-proceedings of the 18th International Workshop on Languages and Compilers for Parallel Computing, LCPC 2005, held in Hawthorne, NY, USA in October 2005. The 26 revised full papers and eight short papers presented were carefully selected during two rounds of reviewing and improvement. The papers are organized in topical sections.

Revisiting Graph Coloring Register Allocation: A Study of the Chaitin-Briggs and Callahan-Koblenz Algorithms.- Register Pressure in Software-Pipelined Loop Nests: Fast Computation and Impact on Architecture Design.- Manipulating MAXLIVE for Spill-Free Register Allocation.- Optimizing Packet Accesses for a Domain Specific Language on Network Processors.- Array Replication to Increase Parallelism in Applications Mapped to Configurable Architectures.- Generation of Control and Data Flow Graphs from Scheduled and Pipelined Assembly Code.- Applying Data Copy to Improve Memory Performance of General Array Computations.- A Cache-Conscious Profitability Model for Empirical Tuning of Loop Fusion.- Optimizing Matrix Multiplication with a Classifier Learning System.- A Language for the Compact Representation of Multiple Program Versions.- Efficient Computation of May-Happen-in-Parallel Information for Concurrent Java Programs.- Evaluating the Impact of Thread Escape Analysis on a Memory Consistency Model-Aware Compiler.- Concurrency Analysis for Parallel Programs with Textually Aligned Barriers.- Titanium Performance and Potential: An NPB Experimental Study.- Efficient Search-Space Pruning for Integrated Fusion and Tiling Transformations.- Automatic Measurement of Instruction Cache Capacity.- Combined ILP and Register Tiling: Analytical Model and Optimization Framework.- Analytic Models and Empirical Search: A Hybrid Approach to Code Optimization.- Testing Speculative Work in a Lazy/Eager Parallel Functional Language.- Loop Selection for Thread-Level Speculation.- Software Thread Level Speculation for the Java Language and Virtual Machine Environment.- Lightweight Monitoring of the Progress of Remotely Executing Computations.- Using Platform-Specific Performance Counters for Dynamic Compilation.- A Domain-Specific Interpreter for Parallelizing a Large Mixed-Language Visualisation Application.- Compiler Control Power Saving Scheme for Multi Core Processors.- Code Transformations for One-Pass Analysis.- Scalable Array SSA and Array Data Flow Analysis.- Interprocedural Symbolic Range Propagation for Optimizing Compilers.- Parallelization of Utility Programs Based on Behavior Phase Analysis.- A Systematic Approach to Model-Guided Empirical Search for Memory Hierarchy Optimization.- An Efficient Approach for Self-scheduling Parallel Loops on Multiprogrammed Parallel Computers.- Dynamic Compilation for Reducing Energy Consumption of I/O-Intensive Applications.- Supporting SELL for High-Performance Computing.- Compiler Supports and Optimizations for PAC VLIW DSP Processors.

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