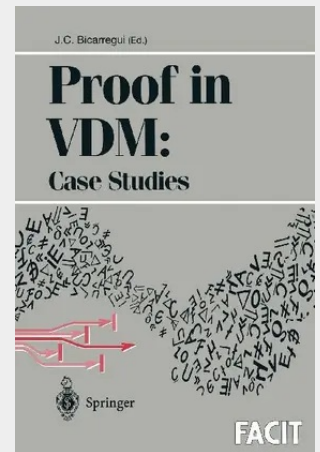


Proof in VDM: Case Studies

Not so many years ago, it would have been difficult to find more than a handful of examples of the use of formal methods in industry. Today however, the industrial application of formal methods is becoming increasingly common in a variety of application areas, particularly those with a safety, security or financially critical aspects. Furthermore, in situations where a particularly high level of assurance is required, formal proof is broadly accepted as being of value. Perhaps the major benefit of formalisation is that it enables formal symbolic manipulation of elements of a design and hence can provide developers with a variety of analyses which facilitate the detection of faults. Proof is just one of these possible formal activities, others, such as test case generation and animation, have also been shown to be effective bug finders. Proof can be used for both validation and verification. Validation of a specification can be achieved by proving formal statements conjectured about the required behaviours of the system. Verification of the correctness of successive designs can be achieved by proof of a prescribed set of proof obligations generated from the specifications.

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106,99 €

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Lieferfrist: bis zu 10 Tage

Artikelnummer: 9783540761860

Medium: Buch

ISBN: 978-3-540-76186-0

Verlag: Springer

Erscheinungstermin: 02.03.1998

Sprache(n): Englisch

Auflage: 1. Auflage. 1998

Serie: Formal Approaches to Computing and Information Technology (FACIT)

Produktform: Kartoniert

Gewicht: 376 g

Seiten: 226

Format (B x H): 155 x 235 mm

