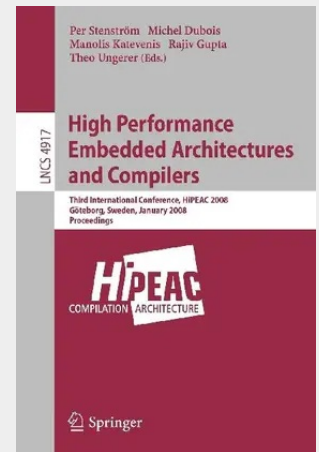


High Performance Embedded Architectures and Compilers

Third International Conference, HiPEAC 2008, Göteborg, Sweden, January 27-29, 2008, Proceedings

This highly relevant and up-to-the-minute book constitutes the refereed proceedings of the Third International Conference on High Performance Embedded Architectures and Compilers, HiPEAC 2008, held in Göteborg, Sweden, January 27-29, 2008. The 25 revised full papers presented together with 1 invited keynote paper were carefully reviewed and selected from 77 submissions. The papers are organized into topical sections on a number of key subjects in the field.

Invited Program.- Supercomputing for the Future, Supercomputing from the Past (Keynote).- I Multithreaded and Multicore Processors.- MIPS MT: A Multithreaded RISC Architecture for Embedded Real-Time Processing.- rMPI: Message Passing on Multicore Processors with On-Chip Interconnect.- Modeling Multigrain Parallelism on Heterogeneous Multi-core Processors: A Case Study of the Cell BE.- IIa Reconfigurable - ASIP.- BRAM-LUT Tradeoff on a Polymorphic DES Design.- Architecture Enhancements for the ADRES Coarse-Grained Reconfigurable Array.- Implementation of an UWB Impulse-Radio Acquisition and Despreading Algorithm on a Low Power ASIP.- IIb Compiler Optimizations.- Fast Bounds Checking Using Debug Register.- Studying Compiler Optimizations on Superscalar Processors Through Interval Analysis.- An Experimental Environment Validating the Suitability of CLI as an Effective Deployment Format for Embedded Systems.- III Industrial Processors and Application Parallelization.- Compilation Strategies for Reducing Code Size on a VLIW Processor with Variable Length Instructions.- Experiences with Parallelizing a Bio-informatics Program on the Cell BE.- Drug Design Issues on the Cell BE.- IV Power-Aware Techniques.- Coffee: COmpiler Framework for Energy-Aware Exploration.- Integrated CPU Cache Power Management in Multiple Clock Domain Processors.- Variation-Aware Software Techniques for Cache Leakage Reduction Using Value-Dependence of SRAM Leakage Due to Within-Die Process Variation.- V High-Performance Processors.- The Significance of Affectors and Affectees Correlations for Branch Prediction.- Turbo-ROB: A Low Cost Checkpoint/Restore Accelerator.- LPA: A First Approach to the Loop Processor Architecture.- VI Profiles: Collection and Analysis.- Complementing Missing and Inaccurate Profiling Using a Minimum Cost Circulation Algorithm.- Using Dynamic Binary Instrumentation to Generate Multi-platform SimPoints: Methodology and Accuracy.- Phase Complexity Surfaces: Characterizing Time-Varying Program Behavior.- VII Optimizing Memory Performance.- MLP-Aware Dynamic Cache Partitioning.- Compiler Techniques for Reducing Data Cache Miss Rate on a Multithreaded Architecture.- Code Arrangement of Embedded Java Virtual Machine for NAND Flash Memory.- Aggressive Function Inlining: Preventing Loop Blockings in the Instruction Cache.



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