Svensson / Monteiro

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation

18th International Workshop, PATMOS 2008, Lisbon, Portugal, September 10-12, 2008, Revised Selected Papers

Welcome to the proceedings of PATMOS 2008, the 18th in a series of int- national workshops. PATMOS 2008 was organized by INESC-ID / IST - TU Lisbon, Portugal, with sponsorship by Cadence, IBM, Chipidea, and Tecmic, and technical co-sponsorship by the IEEE. Over the years, PATMOS has evolved into an important European event, where researchers from both industry and academia discuss and investigate the emerging challenges in future and contemporary applications, design meth- ologies, and tools required for the development of the upcoming generations of integrated circuits and systems. The technical program of PATMOS 2008 c- tained state-of-the-art technical contributions, three invited talks, and a special session on recon?gurable architectures. The technical program focused on t- ing, performance and power consumption, as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis and op- mization in the nanometer era. The Technical Program Committee, with the assistance of additional expert reviewers, selected the 41 papers presented at PATMOS. The papers were - ganized into 7 oral sessions (with a total of 31 papers) and 2 poster sessions (with a total of 10 papers). As is customary for the PATMOS workshops, full papers were required for review, and a minimum of three reviews were received per manuscript.

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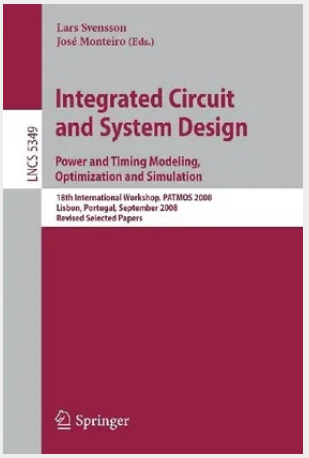

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