

Transactions on High-Performance Embedded Architectures and Compilers IV

Transactions on HiPEAC aims at the timely dissemination of research contributions in computer architecture and compilation methods for high-performance embedded computer systems. Recognizing the convergence of embedded and general-purpose computer systems, this journal publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases. The scope of the journal therefore covers all aspects of computer architecture, code generation and compiler optimization methods of interest to researchers and practitioners designing future embedded systems. This 4th issue contains 21 papers carefully reviewed and selected out of numerous submissions and is divided in four sections. The first section contains five regular papers. The second section consists of the top four papers from the 4th International Conference on High-Performance Embedded Architectures and Compilers, HiPEAC 2009, held in Paphos, Cyprus, in January 2009. The third section contains a set of six papers providing a snap-shot from the Workshop on Software and Hardware Challenges of Manycore Platforms, SHCMP 2008 held in Beijing, China, in June 2008. The fourth section consists of six papers from the 8th IEEE International Symposium on Systems, Architectures, Modeling and Simulation, SAMOS VIII (2008) held in Samos, Greece, in July 2008.

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