

CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications

The intention of this book is to address a number of timely, performance-critical issues within the field of short-distance optical communications, from a circuit designer's perspective. It discusses the major trade-offs the designer has to deal with in the development of monolithically integrated receivers in CMOS technologies. As such, it is based on Dr. Muller's doctoral dissertation entitled "A Standard CMOS Multi-Channel Single-Chip Receiver for Multi-Gigabit Optical Data Communications", submitted to the School of Engineering of the École Polytechnique Fédérale de Lausanne (EPFL) in May 2006. The dissertation material has been enhanced by the presentation of a number of alternative design approaches and circuit topologies, providing exhaustive coverage of the state of the art in optical short-distance receiver circuit design. The need for a new processor input/output (I/O) interface paradigm is dictated by ongoing technology scaling and the advent of multi-core systems. Indeed, each new generation of microprocessors and digital signal processors provides higher computing power and data throughput, whereas the available bandwidth of the I/O interfaces is subject to much slower growth. Moving beyond - coming serial links to an optical data link paradigm for very short-distance (board-to-board and chip-to-chip) communications allows for considerable I/O interface bandwidth enhancement. Fully integrated silicon CMOS receivers are considered to be the technology of choice to lead this solution to economic success, because monolithic integration results in lower volume-manufacturing cost, improved yield and reduced assembly and test expenses.

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