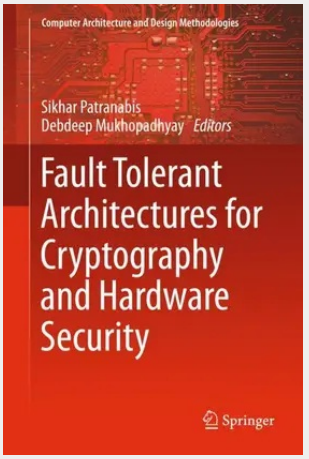
PATRANABIS / Mukhopadhyay

Fault Tolerant Architectures for Cryptography and Hardware Security



This book uses motivating examples and real-life attack scenarios to introduce readers to the general concept of fault attacks in cryptography. It offers insights into how the fault tolerance theories developed in the book can actually be implemented, with a particular focus on a wide spectrum of fault models and practical fault injection techniques, ranging from simple, low-cost techniques to high-end equipment-based methods. It then individually examines fault attack vulnerabilities in symmetric, asymmetric and authenticated encryption systems. This is followed by extensive coverage of countermeasure techniques and fault tolerant architectures that attempt to thwart such vulnerabilities. Lastly, it presents a case study of a comprehensive FPGA-based fault tolerant architecture for AES-128, which brings together of a number of the fault tolerance techniques presented. It concludes with a discussion on how fault tolerance can be combined with side channel security to achieve protection against implementation-based attacks. The text is supported by illustrative diagrams, algorithms, tables and diagrams presenting real-world experimental results.

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